Calculator Structure

Component
École Nationale Supérieure d'Électrotechnique d'Électronique d'Informatique d'Hydraulique et des Télécommunications

Semester
Printemps

In brief

- **Code:** N6AE01C
- **Open to exchange students:** No

Presentation

Objectives

- Emulate the internal operation of a microprocessor associated with its peripherals

- Visualize the flow of information within the architecture and analyze memory accesses

- Develop programs from a set of instructions implemented in the sequencer

Description

Implementation of a minimal computer system based on an EROS (Etude Rationnelle d'un Ordinateur par Simulation) interface with instruction sequencing analysis and assembly language programming with input/output control.

Pre-requisites

minimal system architecture, Von Neumann architecture, sequential and combinatorial logic, input/output interfaces