Verification

🏛 **Component**
École Nationale Supérieure d'Électrotechnique d'Électronique d'Informatique d'Hydraulique et des Télécommunications

In brief

> **Ametys Code:** ELP7

> **Open to exchange students:** Yes

Presentation

Objectives

- Understand the challenges of digital circuit verification (reliability requirements coupled with increasing circuit complexity).

- Understand and implement digital electronic circuit verification techniques in projects (assertions, code coverage, formal verification, etc.).

- Know how to identify the limitations of verification.

Description

The course comprises 3.5 hours of lectures and 10.5 hours of project work, and is assessed through a project report.

The lectures present the concepts described in the learning objectives from a theoretical perspective.

The project allows students to put these concepts into practice by verifying an electronic circuit in which errors were intentionally introduced during the design phase.

Pre-requisites

- Proficiency in VHDL

- Experience in the design of synchronous digital systems.